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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/773,754	02/02/2001	Ming-Dou Ker	H000039	6902

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EXAMINER	
SEFER, AHMED N	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 11/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/773,754	KER ET AL.	
	Examiner	Art Unit	
	A. Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

P riod for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2,4,7,9,11 and 14* is/are allowed.

6)☒ Claim(s) *1,3,5,6,8,10,12,13,15,17 and 19* is/are rejected.

7)☒ Claim(s) *16 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. The amendment filed on 7/15/2003 has been entered; no new claims have been added.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

3. Claims 1 and 3 are rejected under 35 U.S.C. 102(e) as being anticipated by Ker et al. USPN 6,566,715.

Ker et al disclose in figs. 5 and 11 a semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit comprising a substrate of a first conductivity type forming a base for said semiconductor structure; a first region 36 of a second conductivity type within said substrate for forming a drain of a first MOS transistor; a second region 38 of the second conductivity type within said substrate for forming a source of the first MOS transistor; a third region 36 of the second conductivity type for forming a source of a second MOS transistor, wherein a fourth region 40 of the first conductivity type is disposed between the second region of said first MOS transistor and the third region of said

second MOS transistor for surrounding said first MOS transistor with an additional pick-up diffusion to restrain a turn-on of said first MOS transistor.

Regarding claim 3, Ker et al disclose a pre-buffer circuit 70 coupled to a gate of the first MOS transistor Mn3; and an outpad 68 coupled to said first region of the first MOS transistor.

4. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Lee et al. USPN 6,097,066.

Lee et al disclose in fig. 6 a semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit comprising a substrate of a first conductivity type forming a base for said semiconductor structure; a first region 510 of a second conductivity type within said substrate for forming a drain of a first MOS transistor; a second region 530 of the second conductivity type within said substrate for forming a source of the first MOS transistor; a third region 530 of the second conductivity type for forming a source of a second MOS transistor, wherein a fourth region 550 of the first conductivity type is disposed between the second region of said first MOS transistor and the third region of said second MOS transistor for surrounding said first MOS transistor with an additional pick-up diffusion to restrain a turn-on of said first MOS transistor.

5. Claim 5 is rejected under 35 U.S.C. 102(e) as being anticipated by Hsu et al. US Patent No. 6,057,579.

Hsu et al disclose (see figs. 4 and 5, col. 4, lines 19-34) a semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit comprising a substrate of a first conductivity type forming a base for said semiconductor structure; a pair of first regions 408/412 of a second conductivity type within said substrate for

defining a first channel region 428 of the second conductivity type for a first MOS transistor; and a pair of second regions 412/410 of a second conductivity type within said substrate for defining a second channel region 428 of the second conductivity type for a second MOS transistor, wherein the channel length of said first channel region is greater than the channel length of said second channel region.

As for reducing a turn-on speed of said first MOS transistor, a recitation of an intended function of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See In re Casey, 152 USPQ 235 (CCPA 1967) and In re Otto, 136 USPQ 458, 459 (CCPA 1963).

6. Claims 8 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Ker et al. USPN 6,566,715.

Ker et al disclose in figs. 5 and 11 a semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit comprising a p-type substrate of forming a base for said semiconductor structure; a first N+ region 36 within said substrate for forming a drain of a first MOS transistor; a second N+ region 38 within said substrate for forming a source of the first MOS transistor; a third N+ region 36 within said substrate for forming a source of a second MOS transistor, wherein a P+ region 40 is disposed between the second N+ region of said first MOS transistor and the third N+ region of the second MOS transistor for surrounding said first MOS transistor with an additional pick-up diffusion to restrain a turn-on of said first MOS transistor.

Regarding claim 10, Ker et al disclose a pre-buffer circuit 70 coupled to a gate of the first MOS transistor Mn3; and an outpad 68 coupled to said first region of the first MOS transistor.

7. Claim 8 is rejected under 35 U.S.C. 102(e) as being anticipated by Lee et al. USPN 6,097,066.

Lee et al disclose in fig. 5 a semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit comprising a p-type substrate of forming a base for said semiconductor structure; a first N+ region 510 within said substrate for forming a drain of a first MOS transistor; a second N+ region 530 within said substrate for forming a source of the first MOS transistor; a third N+ region 530 within said substrate for forming a source of a second MOS transistor, wherein a P+ region 550 is disposed between the second N+ region of said first MOS transistor and the third N+ region of the second MOS transistor for surrounding said first MOS transistor with an additional pick-up diffusion to restrain a turn-on of said first MOS transistor.

8. Claim 12 is rejected under 35 U.S.C. 102(e) as being anticipated by Ker et al. USPN 6,072,219.

Ker et al discloses (see figs. 8 and 9 and claims 6 and 7) a semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit comprising a p-type substrate forming a base for said semiconductor structure; a pair of first N+ regions 62 within said substrate for defining a first n-channel region for a first MOS transistor N2; and a pair of second N+ regions 52 within said substrate for defining a second n-channel region for a second MOS transistor N1, wherein the channel length of a first MOS transistor longer than a second MOS transistor.

9. Claim 15 is rejected under 35 U.S.C. 102(e) as being anticipated by Lin et al. USPN 6,559,508.

Lin et al. disclose figs. 1-6 a semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit, said semiconductor structure connected between an input pad 11 and an internal circuit of said integrated circuit comprising a substrate 40 of a first conductivity forming a base for said semiconductor structure; a first channel 24 formed between a pair of first regions 22/25 of a second conductivity type within said substrate for a first MOS transistor; and a second channel 24 formed between a pair of second regions 22/25 of a second conductivity type within said substrate for a second MOS transistor, wherein an additional pick-up diffusion region 20 is disposed between the source region of said first regions and the source region of said second regions for surrounding said first MOS transistor with an additional pick-up diffusion to restrain the turn-on of said first MOS transistor.

10. Claim 17 is rejected under 35 U.S.C. 102(e) as being anticipated by Lin et al. USPN 6,559,508.

Lin et al disclose in figs. 1-7 a semiconductor structure for electrostatic discharge (ESD) protection of a high-voltage tolerant I/O cells with stacked NMOS integrated circuits, said semiconductor structure connected between a pre-driver circuit 13 and input/output pad 11 of said integrated circuit and comprising a substrate of first conductivity forming a base for said semiconductor structure; a first channel 24 formed between a pair of first regions 22/25 of a second conductivity type within said substrate for a first MOS transistor which is stacked on a third MOSFET of a second conductivity type; and a second channel 27 formed between a pair of

second regions 25/28 of a second conductivity type within said substrate for a second MOS transistor which is stacked on a fourth MOSFET of a second conductivity type, wherein an additional pick-up diffusion region 20 is disposed between the source region of said first regions and the source region of said second regions for surrounding said first MOS transistor with an additional pick-up diffusion to restrain the turn-on of said first MOS transistor.

11. Claim 19 is rejected under 35 U.S.C. 102(e) as being anticipated by Lin et al. / Ker et al./Lee et al.

Lin et al/ Ker et al/Lee et al disclose a semiconductor structure for electrostatic discharge (ESD) protection comprising at least one ESD protection device; and at least one guarded device which is turned –on by a turn-on restrained means, wherein the ESD protection device can be turned-on before the turn-on restrained means is turned on.

12. Claim 19 is rejected under 35 U.S.C. 102(e) as being anticipated by Maria Verhaege et al. US PG-Pub 2002/0033507.

Maria Verhaege et al disclose (see par. 0085) a semiconductor structure for electrostatic discharge (ESD) protection comprising at least one ESD protection device; and at least one guarded device which is turned–on by a turn-on restrained means, wherein the ESD protection device can be turned-on before the turn-on restrained means is turned on.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al.

Hsu et al disclose (see figs. 4 and 5, col. 4, lines 3-34) a semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit comprising a substrate forming a base for said semiconductor structure; a pair of first regions 412/408 within said substrate for defining a first channel region 428 for a first MOS transistor; and a pair of second regions 410/412 within said substrate for defining a second channel region 428 for a second MOS transistor, wherein the channel length of a first MOS transistor longer than a second MOS transistor, but do not specifically disclose a p-type substrate or a pair of first and second N+ regions. It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ p-type substrate and a pair of first and second N+ regions forming first and second n-channels respectively.

14. Claims 6 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. in view of admitted prior art (APA).

Hsu et al disclose all the claimed subject matter but fail to disclose a pre-puffer circuit coupled to a channel and an output pad coupled to a first region or regions of a MOS transistor.

The APA disclose in figs. 2-5 a pre-puffer coupled to a gate of a MOS transistor or to a channel; and an output pad coupled to a region or regions of a MOS transistor.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate the teachings of the APA with Hsu et al, since that would reduce transient contributions to a response.

Allowable Subject Matter

15. Claims 2, 4, 7, 9, 11 and 14 are allowed.

16. Claims 16 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (703) 605-1227.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601.

ANS
October 27, 2003

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
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